

What is claimed is:

1. A flipflop, comprising:
 - 2 a differential pair comprising a first transistor
 - 3 and a second transistor, wherein control
 - 4 terminals of the first and second transistors
 - 5 are coupled to a first input signal and a
 - 6 second input signal respectively, and first
 - 7 terminals of the first and second transistors
 - 8 are coupled to a common node;
 - 9 a first latch unit coupled between the common node
 - 10 and a first voltage, and connected to the
 - 11 differential pair in parallel, comprising a
 - 12 first node and a second node to respectively
 - 13 coupled to second terminals of the first and
 - 14 second transistors in the differential pair
 - 15 to generate complementary latch signals
 - 16 according to the first and second input
 - 17 signals;
 - 18 a signal amplification circuit coupled to the
 - 19 differential pair and the first latch unit,
 - 20 comprising a first control terminal coupled
 - 21 to a control signal, to generate
 - 22 complementary amplified signals according to
 - 23 the complementary latch signals; and
 - 24 a second latch unit coupled to the signal amplifier
 - 25 circuit to generate complementary static
 - 26 output signals according to the complementary
 - 27 amplified signals and to maintain the

28 complementary static output signals, wherein
29 the first input signal is the inverse of the
30 second input signal.

1 2. The flipflop as claimed in Claim 1, wherein the
2 signal amplification circuit further comprises second and
3 third control terminals coupled to the first input signal and
4 the second input signal respectively.

1 3. The flipflop as claimed in Claim 2, wherein the
2 first latch unit comprises:

3 a first inverter comprising an input terminal coupled
4 to the second node, and an output terminal; and
5 a second inverter cross-coupled to the first inverter,
6 comprising an input terminal coupled to the first
7 node and the output terminal of the first inverter,
8 and an output terminal coupled to the output
9 terminal of the first inverter and the second node.

1 4. The flipflop as claimed in Claim 2, further
2 comprising a current source transistor coupled between the
3 common node and a second voltage, and comprising a control
4 terminal coupled to the control signal.

1 5. The flipflop as claimed in Claim 4, wherein the
2 differential circuit further comprises:

3 a third transistor coupled between the first voltage and
4 the first node comprising a control terminal
5 coupled to the control signal; and

6 a fourth transistor coupled between the first voltage
7 and the second node comprising a control terminal
8 coupled to the control signal.

1 6. The flipflop as claimed in Claim 5, wherein the
2 second latch unit comprises:

3 a third inverter comprising an input terminal and an
4 output terminal; and

5 a fourth inverter cross-coupled to the fourth inverter,
6 comprising an input terminal and an output terminal
7 coupled to the output terminal and the input
8 terminal of the third inverter respectively,
9 wherein the input terminals of the third and fourth
10 inverters are coupled to the complementary
11 amplified signals respectively.

1 7. The flipflop as claimed in Claim 6, wherein the
2 signal amplification circuit comprises:

3 a fifth inverter coupled to the first voltage and
4 comprising an input terminal coupled to the first
5 node;

6 a fifth transistor comprising a first terminal coupled
7 to the fifth inverter, a control terminal coupled
8 to the control terminal of the second transistor,
9 and a second terminal;

10 a sixth transistor comprising a first terminal coupled
11 to the second terminal of the fifth transistor, a
12 second terminal coupled to the second voltage, and
13 a control terminal coupled to the control signal;

14 a sixth inverter coupled to the first voltage and
15 comprising an input terminal coupled to the second
16 node;

17 a seventh transistor comprising a first terminal coupled
18 to the sixth inverter, a control terminal coupled
19 to the control terminal of the first transistor,
20 and a second terminal; and

21 an eighth transistor comprising a first terminal coupled
22 to the second terminal of the seventh transistor,
23 a control terminal coupled to the control signal,
24 and a second terminal coupled to the second
25 voltage.

8. The flipflop as claimed in Claim 6, wherein the signal amplification circuit comprises:

a fifth transistor comprising a first terminal coupled to the first voltage, a control terminal coupled to first node, and a second terminal;

a sixth transistor comprising a first terminal coupled to the second terminal of the fifth transistor, a control terminal coupled to the control terminal of the second transistor, and a second terminal;

a seventh transistor comprising a first terminal coupled to the second terminal of the sixth transistor, a second terminal coupled to the second voltage and a control terminal coupled to the control signal;

an eighth transistor comprising a first terminal coupled to the first voltage, a control terminal coupled to the second node, and a second terminal;

17 a ninth transistor comprising a first terminal coupled
18 to the second terminal coupled to the eighth
19 transistor, a control terminal coupled to the
20 control terminal of the first transistor, and a
21 second terminal; and
22 a tenth transistor comprising a first terminal coupled
23 to the second terminal of the ninth transistor, a
24 control terminal coupled to the control signal and
25 a second terminal coupled to the second voltage.

1 9. A flipflop, comprising:

2 a sense amplifier receiving two input signals and
3 outputting complementary latch signals,
4 comprising:

5 a first latch unit coupled between the common node
6 and a first voltage, comprising a first
7 inverter and a second inverter cross-coupled
8 to each other, and comprising a first node and
9 a second node to output the complementary
10 latch signals respectively; and

11 a differential pair comprising a first transistor
12 and a second transistor, connected to the
13 first latch unit in parallel, wherein control
14 terminals of the first and second transistors
15 are coupled to the two input signal
16 respectively;

17 a signal amplification circuit comprising two input
18 terminals coupled to the first node and the second
19 node respectively, a first control terminal

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coupled to a control signal, and two output terminals; and

22 a second latch unit comprising a third node and a fourth
23 node coupled to the two output terminals of the
24 signal amplification circuit.

1 10. The flipflop as claimed in Claim 9, wherein, in the
2 first latch unit, the first inverter comprises an input
3 terminal coupled to an output terminal of the second inverter,
4 serving as the second node, and an output terminal coupled
5 to an input terminal of the second inverter, serving as the
6 first node.

1 11. The flipflop as claimed in Claim 10, wherein, in
2 the differential pair, the first and second transistors
3 comprise first terminals coupled to the first node and the
4 second node of the first latch unit respectively and second
5 terminals coupled to a common node together.

3 a third transistor coupled between the first voltage and
4 the first node of the first latch unit, and
5 comprising a control terminal coupled to the
6 control signal; and

7 a fourth transistor coupled between the first voltage
8 and the second node of the first latch unit, and comprising
9 a control terminal coupled to the control signal.

1 13. The flipflop as claimed in Claim 12, further
2 comprising a current source transistor coupled between the

3 common node and a second voltage, and comprising a control
4 terminal coupled to the control signal.

1 14. The flipflop as claimed in Claim 12, wherein the
2 second latch unit comprises:

3 a third inverter comprising an input terminal and an
4 output terminal; and

5 a fourth inverter cross-coupled to the third inverter,
6 comprising an input terminal coupled to the output
7 terminal of the third inverter, serving as the
8 fourth node, and an output terminal coupled to the
9 input terminal of the third inverter, serving as
10 the third node.

1 15. The flipflop as claimed in Claim 14, wherein the
2 signal amplification circuit comprises:

3 a fifth inverter coupled to the first voltage, comprising
4 an input terminal coupled to the first node and an
5 output terminal coupled to the third node;

6 a fifth transistor comprising a first terminal coupled
7 to the fifth inverter, a control terminal coupled
8 to the control terminal of the second transistor,
9 and a second terminal;

10 a sixth transistor comprising a first terminal coupled
11 to the second terminal of the fifth transistor, a
12 second terminal coupled to the second voltage, and
13 a control terminal coupled to the control signal;

14 a sixth inverter coupled to the first voltage, comprising
15 an input terminal coupled to the second node and
16 an output terminal coupled to the fourth node;

17 a seventh transistor comprising a first terminal coupled
18 to the sixth inverter, a control terminal coupled
19 to the control terminal of the first transistor,
20 and a second terminal; and
21 an eighth transistor comprising a first terminal coupled
22 to the second terminal of the seventh transistor,
23 a control terminal coupled to the control signal,
24 and a second terminal coupled to the second
25 voltage.

1 16. The flipflop as claimed in Claim 14, wherein the
2 signal amplification circuit comprises:

3 a fifth transistor comprising a first terminal coupled
4 to the first voltage, a control terminal coupled
5 to first node, and a second terminal coupled to the
6 third node;

7 a sixth transistor comprising a first terminal coupled
8 to the second terminal of the fifth transistor, a
9 control terminal coupled to the control terminal
10 of the second transistor, and a second terminal;

11 a seventh transistor comprising a first terminal coupled
12 to the second terminal of the sixth transistor, a
13 second terminal coupled to the second voltage and
14 a control terminal coupled to the control signal;

15 an eighth transistor comprising a first terminal coupled
16 to the first voltage, a control terminal coupled
17 to the second node, and a second terminal coupled
18 to the fourth node;

19 a ninth transistor comprising a first terminal coupled
20 to the second terminal coupled to the eighth

21 transistor, a control terminal coupled to the
22 control terminal of the first transistor, and a
23 second terminal; and

24 a tenth transistor comprising a first terminal coupled
25 to the second terminal of the ninth transistor, a
26 control terminal coupled to the control signal and
27 a second terminal coupled to the second voltage.

17. A flipflop, comprising:

2 a first transistor comprising a first terminal coupled
3 to a first voltage, a second terminal coupled to
4 a first node, and a control terminal;

5 a second transistor comprising a first terminal coupled
6 to the first node, a control terminal coupled to
7 the control terminal of the first transistor, and
8 a second terminal coupled to a common node;

9 a third transistor coupled between the first voltage and
10 the first node;

11 a fourth transistor coupled between the first node and
12 the common node, comprising a control terminal
13 coupled to a first input signal;

14 a fifth transistor comprising a first terminal coupled
15 to the first voltage, a second terminal coupled to
16 a second node, and a control terminal coupled to
17 the first node;

18 a sixth transistor comprising a control terminal coupled
19 to the control terminal of the fifth transistor,
20 a first terminal coupled to the second node and the
21 control terminal of the first transistor, and a
22 second terminal coupled to the common node;

23 a seventh transistor coupled between the first voltage
24 and the second node;
25 an eighth transistor coupled between the second node and
26 the common node, comprising a control terminal
27 coupled to a second input signal, wherein the first
28 input signal is inverse of the second input signal;
29 a ninth transistor coupled between the common node and
30 a second voltage, wherein control terminals of the
31 third, seventh and ninth transistors are coupled
32 to a control signal;
33 a signal amplification circuit comprising two input
34 terminals coupled to the first and second node
35 respectively, a first control terminal coupled to
36 the control terminal, a second control terminal and
37 a third control terminal respectively coupled to
38 the second and first input signals, a first output
39 terminal and a second output terminal;
40 a first inverter comprising an input terminal coupled
41 to the first output terminal of the signal
42 amplification circuit, and an output terminal; and
43 a second inverter comprising an input terminal coupled
44 to the second output terminal of the signal
45 amplification circuit, and an output terminal
46 coupled to the output terminal coupled to the
47 output terminal of the first inverter.

18. The flipflop as claimed in Claim 17, the signal amplification circuit comprising;

a tenth transistor comprising a first terminal coupled to the first voltage, a control terminal coupled

5 to the first node, a second terminal as the first
6 output terminal coupled to the input terminal of
7 the first inverter;

8 an eleventh transistor comprising a first terminal
9 coupled to the second terminal of the tenth
10 transistor, a control terminal coupled to the
11 control terminal of first node, and a second
12 terminal;

13 a twelfth transistor comprising a first terminal coupled
14 to the second terminal of the eleventh transistor,
15 a control terminal coupled to the second input
16 signal, and a second terminal;

17 a thirteenth transistor coupled between the second
18 terminal of the twelfth transistor and the second
19 voltage;

20 a fourteenth transistor comprising a first terminal
21 coupled to the first voltage, a control terminal
22 coupled to the second node, and a second terminal
23 as the second output terminal coupled to the input
24 terminal of the second inverter;

25 a fifteenth transistor comprising a first terminal
26 coupled to the second terminal of the fourteenth
27 transistor, a control terminal coupled to the
28 second node, and a second terminal;

29 a sixteenth transistor comprising a first terminal
30 coupled to the second terminal of the fifteenth
31 transistor, a control terminal coupled to the first
32 input signal, and a second terminal; and

33 a seventeenth transistor coupled between the second
34 terminal of the sixteenth transistor and the second
35 voltage, control terminals of the thirteenth and
36 seventeenth transistors, as the first control
37 terminal of the signal amplification circuit,
38 coupled to the control terminal.

1 19. The flipflop as claimed in Claim 17, the signal
2 amplification circuit comprising:

3 a tenth transistor comprising a first terminal coupled
4 to the first voltage, a control terminal coupled
5 to the first node, and second terminal as the first
6 output terminal coupled to the input terminal of
7 the first inverter;

8 an eleventh transistor comprising a first terminal
9 coupled to the second terminal of the tenth
10 transistor, a control terminal coupled to the
11 second input signal, and a second terminal;

12 a twelfth transistor coupled between the second terminal
13 of the eleventh transistor and the second voltage;

14 a thirteenth transistor comprising a first terminal
15 coupled to the first voltage, a control terminal
16 coupled to the second node, and a second terminal
17 as the second output terminal coupled to the input
18 terminal of the second inverter;

19 a fourteenth transistor comprising a first terminal
20 coupled to the second terminal of the thirteenth
21 transistor, a control coupled to the first input
22 signal, and a second terminal; and

23 a fifteenth transistor coupled between the second
24 terminal of the fourteenth transistor and the
25 second voltage, control terminals of the twelfth
26 and fifteenth transistors, as the first control
27 terminal of the signal amplification circuit,
28 coupled to the control signal.